REDUCED GUARD RING IN SCHOTTKY BARRIER DIODE STRUCTURE

DESCRIPTION

[Para 1] FIELD OF THE INVENTION

[Para 2] The invention relates to Schottky barrier diodes and, more particularly, to Schottky barrier diodes using a dielectric separation region to bound an active Schottky junction area to reduce or eliminate parasitic capacitance caused by the use of a guard ring around an anode of an integrated circuit device.

[Para 3] BACKGROUND OF THE INVENTION

[Para 4] Schottky barrier diodes, such as in a rectifier, may involve using a p-type guard ring located at the periphery of the metal electrode. The guard ring may reduce or eliminate edge effects by reducing the electrical field concentrations and by moving the edge of the electrode away from the barrier junction. However, use of a guard ring introduces parasitic capacitance that often must be accounted for when designing a circuit.

[Para 5] In the past, Schottky diode devices have been used in an integrated circuit. A P+ guard ring has been used around the edge of the silicon active region and the isolation oxides. The P+ guard ring was used to improve the reliability of the integrated circuit. For example, a P+ guard ring was formed around the anode of the integrated circuit diode device. However, issues in performance may arise due to the P+ guard ring. More particularly, with a P+ guard ring, the P+ region may act as a landing pad for contacts to land on, and therefore may become part of the device and provide unwanted parasitic capacitance. When the device is used at high frequencies, the parasitic capacitance occurs from the P+ junction down to the sub-collector and plus regions; however, parasitic capacitance may also occur with an N+ junction down to the relevant sub-collector within a P-type Schottky diode structure.

[Para 6] Figs. 1A, 1B and 1C illustrate top, first side and second side views, respectively, of a Schottky barrier diode (SBD) in a conventional embodiment. The SBD 100 includes cathodes 102 having cathode contacts 104, and an anode 106 having anode contacts 108. Reach-through implants 110 are located beneath the cathodes 104. A sub-collector 112 is located so as to be connected to both reach through implants 110 and serves as the actual devices cathode region. A guard ring 114 implant region is provided on the periphery of the anode 106 to reduce current leakage, improve reliability and eliminate current crowding. However, the guard ring 114 may introduce parasitic capacitance from its P+ region to the N+ sub-collector. Parasitic capacitance may be of particular issue at higher frequencies, *e.g.*, frequencies greater than 50 GHz.

[Para 7] SUMMARY OF THE INVENTION

[Para 8] According to an exemplary embodiment of the invention, a Schottky barrier diode includes an active area, at least one separation region bounding the active area, and an electrode formed in the active area to form a Schottky junction, wherein the at least one separation region reduces parasitic capacitance about the Schottky junction.

[Para 9] According to a further exemplary embodiment of the invention, a Schottky barrier diode includes a semiconductor substrate, at least one separation region bounding an active area formed on the semiconductor substrate, a portion of a guard ring on the substrate, and an electrode formed on a surface of the semiconductor substrate in the active area to form a Schottky junction, wherein the at least one separation region reduces parasitic capacitance about the Schottky junction, and the separation region is substantially formed in the active region to eliminate other portions of the guard ring at the portion where the at least one separation region is located.

[Para 10] According to another exemplary embodiment of the invention, a process for forming a Schottky barrier diode, includes the steps of forming an active area in a substrate, forming an electrode on the substrate in the active area to form a Schottky junction, and forming at least one separation region

on the substrate where the at least one separation region is bounded on one side by the active area, wherein the at least one separation region reduces parasitic capacitance about the Schottky junction.

[Para 11] BRIEF DESCRIPTION OF THE DRAWINGS

[Para 12] The above and other features and advantages of the invention will become more apparent to those of ordinary skill in the art by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

[Para 13] Figs. 1A, 1B and 1C illustrate top, first side and second side views, respectively, of a Schottky barrier diode in a conventional embodiment;

[Para 14] Fig. 2A illustrates a top view of a Schottky barrier diode structure according to an embodiment of the invention;

[Para 15] Fig. 2B illustrates a side view of an embodiment of the invention along line B-B in Fig. 2A;

[Para 16] Fig. 2C illustrates a side view of an embodiment of the invention along line C-C in Fig. 2A;

[Para 17] Fig. 3A, illustrates a top view of a Schottky barrier diode structure according to an embodiment of the invention;

[Para 18] Fig. 3B illustrates a side view of an embodiment of the invention along line B-B of Fig. 3A;

[Para 19] Fig. 3C illustrates a side view of an embodiment of the invention along line C-C in Fig. 3A;

[Para 20] Fig. 4A illustrates a top view of a Schottky barrier diode structure according to an embodiment of the invention;

[Para 21] Fig. 4B illustrates a side view of an embodiment of the invention along line B-B of Fig. 4A;

[Para 22] Fig. 4C illustrates a side view of an embodiment of the invention along line C-C of Fig. 4A;

[Para 23] Fig. 5 illustrates a top view of a Schottky barrier diode structure according to an embodiment of the invention; and

[Para 24] Fig. 6 is a flowchart illustrating a method of making a Schottky barrier diode structure according to an embodiment of the invention.

[Para 25] DETAILED DESCRIPTION OF

[Para 26] EMBODIMENTS OF THE INVENTION

[Para 27] The invention relates to Schottky barrier diodes using a dielectric separation region to bound an active region, which thus eliminates at least a portion of a guard ring in at least one dimension. As described hereinafter, a guard ring is referred to as a non-closed loop landing pad of a p-type (or n-type) region. Thus, the guard ring is disjointed, in that it is not a connected or closed ring. The guard ring will be used to reduce current leakage, improve reliability, eliminate current crowding and act as a landing pad region for contacts. Although the present invention is directed to eliminating a portion of such a guard ring, the use of the term guard ring will continue to be used to indicate a structure for performing such functions, even when the structure is not in the shape of a ring. According to an embodiment of the invention, the use of a P+ guard ring may be reduced or eliminated by employing the separation region. This may allow the reduction or elimination of parasitic capacitance in the integrated circuit device. The separation region, which may be a dielectric, may be formed in an active region of the SBD. This separation region eliminates regions of the guard ring in one or two dimensions.

[Para 28] Fig. 2A illustrates a top view of a Schottky barrier diode structures according to an embodiment of the invention. The SBD 200 includes cathodes 202 having cathode contacts 204, and an anode 206 having anode contacts 208. Reach through implants 210 are located beneath the cathodes 204. A sub-collector 212 is located so as to be connected to both reach through implants 210. A portion of guard ring 214 is provided between a portion of

the cathodes 202 and the anode 206. However, a separation region 216 is provided to replace other portions of guard ring 214 in one dimension.

[Para 29] Separation region 216 may be an insulator to reduce current leakage, improve reliability and eliminate current crowding, as well as reduce or eliminate parasitic capacitance. Thus, the P+ parasitic capacitance may be reduced or eliminated in the x-direction. In one embodiment of the invention, separation region 216 is provided in one dimension, thereby replacing that portion of the guard ring 214. Thus, the guard ring is disjointed, in that it is not a connected or closed ring.

[Para 30] Fig. 2B illustrates a side view of an embodiment of the invention along line B-B in Fig. 2A. Separation region 216 is shown in one dimension. Reach through implants 210 are adjacent to the sub-collector 212. Sub-collector 212 is located generally below separation region 216.

[Para 31] Fig. 2C illustrates a side view of an embodiment of the invention along line C-C in Fig. 2A. A portion of guard ring 214 is shown in one dimension. Sub-collector 212 is located generally below guard ring 214.

[Para 32] Fig. 3A illustrates a top view of a Schottky barrier diode structure according to an embodiment of the invention. The SBD 300 includes cathodes 302 having cathode contacts 304, and an anode 306 having anode contacts 308. Reach through implants 310 are located beneath the cathodes 304. A sub-collector 312 is located so as to be connected to both reach through implants 310. A portion of a guard ring 314 is provided between the cathodes 302 and the anode 306. However, separation region 316 is provided to replace a portion of guard ring 314 in one dimension. Thus, the P+ parasitic capacitance may be reduced or eliminated in the y-direction. In one embodiment of the invention, separation region 316 is provided in one dimension, thereby replacing that portion of the implanted guard ring 314. Thus, the guard ring is disjointed, in that it is not a connected or closed ring.

[Para 33] Fig. 3B illustrates a side view of an embodiment of the invention along line B-B in Fig. 3A. Reach through implants 310 are adjacent to the

sub-collector 312. A portion of guard ring 314 is shown in one dimension. Sub-collector 312 is located generally below guard ring 314.

[Para 34] Fig. 3C illustrates a side view of an embodiment of the invention along line C-C in Fig. 3A. Separation region 316 is shown in one dimension. Sub-collector 312 is located generally below separation region 316.

[Para 35] According to an embodiment of the invention, parasitic capacitance from the guard ring may be reduced or eliminated by using a nitride thin film layer in the separation region 216, 316 in the standard CMOS or standard integrated circuit device technology. For example, a nitride, an oxide, a polymer and/or a glass material may be used to build a resistor or other insulating non-conductive structure. According to an exemplary embodiment of the invention, the separation region 216, 316 is a dielectric, such as that used for resistors, placed at the end of the front end of line (FEOL) process of the integrated circuit to block the silicide formation on the silicon in that region. In this manner, a nitride layer placed in this position in a diode integrated circuit device moves the Schottky junction away from that edge, thereby allowing a portion of the guard ring to be eliminated.

[Para 36] Once the separation region 216, 316, such as a nitride layer, is placed down, the integrated circuit device is etched using any conventional etching process. A standard silicidation process is performed, so that the silicide is formed everywhere that the silicon is exposed and not formed under the nitride layer. By using the nitride layer, the P+ guard ring may be eliminated in at least one dimension in such areas.

[Para 37] Thus, the nitride layer may be used to prevent the metallurgical junction from being formed all the way to the edge of the diode device, thereby enabling the elimination of at least a portion of the P+ guard ring.

[Para 38] Accordingly, in embodiments of the invention, a portion of the guard ring is maintained at least in a portion of the integrated circuit device to act as a landing pad region for the contacts connected to the anode of the Schottky barrier diode device. As shown in Figs. 2A-2C and 3A-3C, the

separation layer or region 216, 316 eliminates other portions of the guard ring in one dimension. Also, according to another embodiment of the invention, a guard ring may be completely omitted from the SBD (which can be represented by any Figs. 2A - 4C). In such an embodiment, the separation layer or region is formed in two dimensions.

[Para 39] As shown in the figures and now understood in view of the disclosures, the device is a Schottky diode with a Schottky junction. The location of the Schottky junction is based in part on the configuration of the diode structure, the materials used, and the like. Based on the configurations described in various embodiments of the invention, the separation region reduces parasitic capacitance about the Schottky junction. Further, the edge of the Schottky junction may be spaced away from the isolation region bounding the active Si area.

[Para 40] Figs. 4A-4C illustrate an embodiment with the P+ guard ring located away from the active part of the device. Therefore, the device may include a portion of the guard ring while reducing or eliminating parasitic capacitance from the P+ to the N+ region. Distance d_{sc-gr} is the distance between the sub-collector region and the guard ring. The distance d_{sc-gr} may be varied to control, reduce or eliminate the parasitic capacitance in the device. According to an embodiment of the invention, the distance d_{sc-gr} may be far enough to reduce the parasitic capacitance but close enough to allow the guard ring to cover the contacts. This distance may vary based on, among other criteria, the type of sub-collector used, the integrated circuit device, the materials, the doping levels, and the like.

[Para 41] In particular, Fig. 4A illustrates a top view of a Schottky barrier diode structure according to an embodiment of the invention. The SBD 400 includes cathodes 402 having cathode contacts 404, and an anode 406 having anode contacts 408. Reach through implants 410 are located beneath the cathodes 404. A sub-collector 412 is located so as to be connected to both reach through implants 410. A portion of a guard ring 414 is provided between the cathodes 402 and the anode 406.

[Para 42] In this embodiment, separation region 416 is provided to isolate the anode 406 Schottky junction from the isolation or shallow trench isolation edge. In one embodiment of the invention, separation region 416 is provided in one dimension, thereby replacing that portion of the guard ring 414. Thus, the guard ring 414 is disjointed, in that it is not a connected or closed ring. Thus, the P+ capacitance may be reduced or eliminated by the separation region 416 in the x-direction, while the P+ capacitance may be reduced based on distance d_{sc-gr}, discussed below, in the y-direction.

[Para 43] Fig. 4B illustrates a side view of an embodiment of the invention along line B-B in Fig. 4A. Separation region 416 is shown in one dimension. Reach through implants 410 are adjacent to the sub-collector 412. Sub-collector 412 is located generally below separation region 416.

[Para 44] Fig. 4C illustrates a side view of an embodiment of the invention along line C-C in Fig. 4A. A portion of guard ring 414 is shown in one dimension. Sub-collector 412 is located generally below guard ring 414.

[Para 45] The sub-collector 412 may be implanted in devices used for various technologies, such as wireless devices. The deep implanted sub-collector process may result in less lateral diffusion of the dopant, so a sub-collector defined within the guard rings does not diffuse as much laterally as compared to a buried subcollector process. A buried sub-collector process may include implanting the sub-collector, growing a film on top, burying the sub-collector, and annealing the film. The profile of such sub-collector may be such that the dopant concentration is highest in the active region of the device, and gradually lowers so the concentration can be lower underneath at the contact and thus reduce guard ring to subcollector parasitic capacitance.

[Para 46] Fig. 5 illustrates a top view of a Schottky barrier diode structure according to an embodiment of the invention. The SBD 500 includes a cathode 502 having cathode contacts 504, and an anode 506 having anode contacts 508. Reach through implant 510 is located beneath the cathodes 504. A sub-collector 512 is located so as to be connected to the reach through implant 510. A portion of a guard ring 514 is provided on one side of the anode 506.

[Para 47] In this embodiment, separation region 516 is provided to isolate the anodes 506 Schottky junction from the isolation or STI region edge around this active Si region. In one embodiment of the invention, separation region 516 is provided on three sides of the anode 506, thereby replacing those portions of the guard ring 514. Thus, the guard ring 514 is one strip or side, while the separation region 516 is formed in a "U" shape. Thus, the parasitic capacitance may be reduced or eliminated by the separation region 516 in both the x-direction and the y-direction, while the parasitic capacitance may be reduced based on distance d_{sc-gr}, discussed above, in the y-direction. The SBD of Fig. 5 operates in a similar manner to those illustrated in Figs. 2-4.

[Para 48] Fig. 6 is a flowchart illustrating a method of making Schottky barrier diode structures according to an embodiment of the invention. At step 610, an active region is formed in a substrate. With reference to Fig. 4A for illustration, an active region may be a cathode 402 and/or an anode 406 formed in any conventionally known manner.

[Para 49] At step 620, an separation region is formed. As described above, forming the separation region may include placing a dielectric layer, such as nitride, glass, polymer, oxide, or similar material, on the substrate. This may be performed by using any known deposition or appropriate growing method and, if necessary, a planarization step. A silicidation process is then performed on the substrate to provide silicide. The dielectric layer blocks the silicide formation on the substrate, such that the dielectric forms the separation region and reduces or eliminates parasitic capacitance in the integrated circuit device.

[Para 50] At step 630, one or more electrodes are formed in any known manner on the surface of the substrate. This formation completes the Schottky diode, where parasitic capacitance is reduced or eliminated in the resulting integrated circuit device.

[Para 51] While the invention has been described in terms of exemplary embodiments, those skilled in the art will recognize that the invention can be

practiced with modifications and in the spirit and scope of the appended claims.